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**CSE251**

**Electronic Devices and Circuits**

**Semester: Fall 22**

Exp -05: Study of I-V Characteristics of BJT and

Implementation of CE Amplifier Using BJT

**Submitted By**

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Date of performance: 31/10/22

Date of Submission: 21/11/22

**2. Circuit Diagrams:**

Diagram 1:

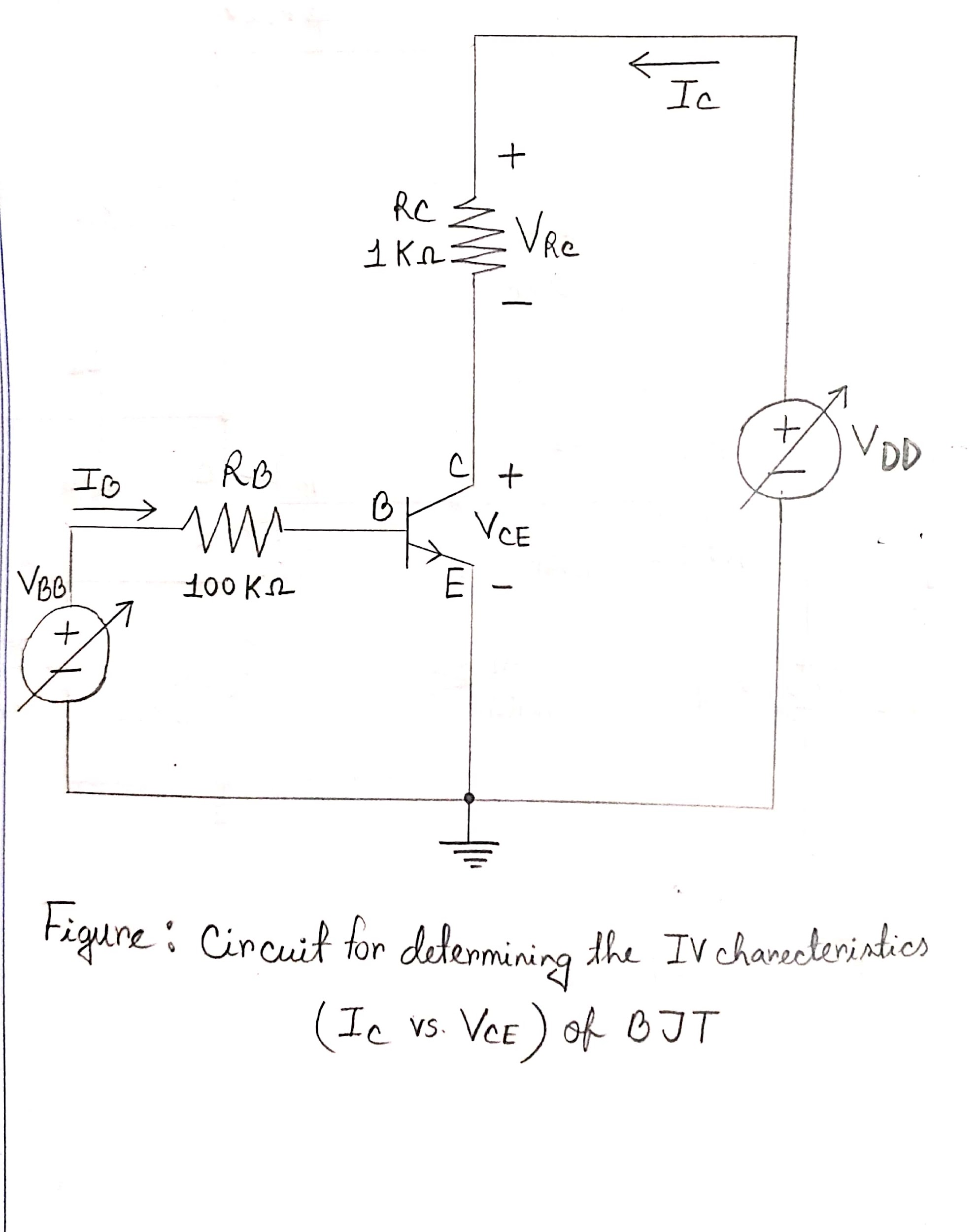
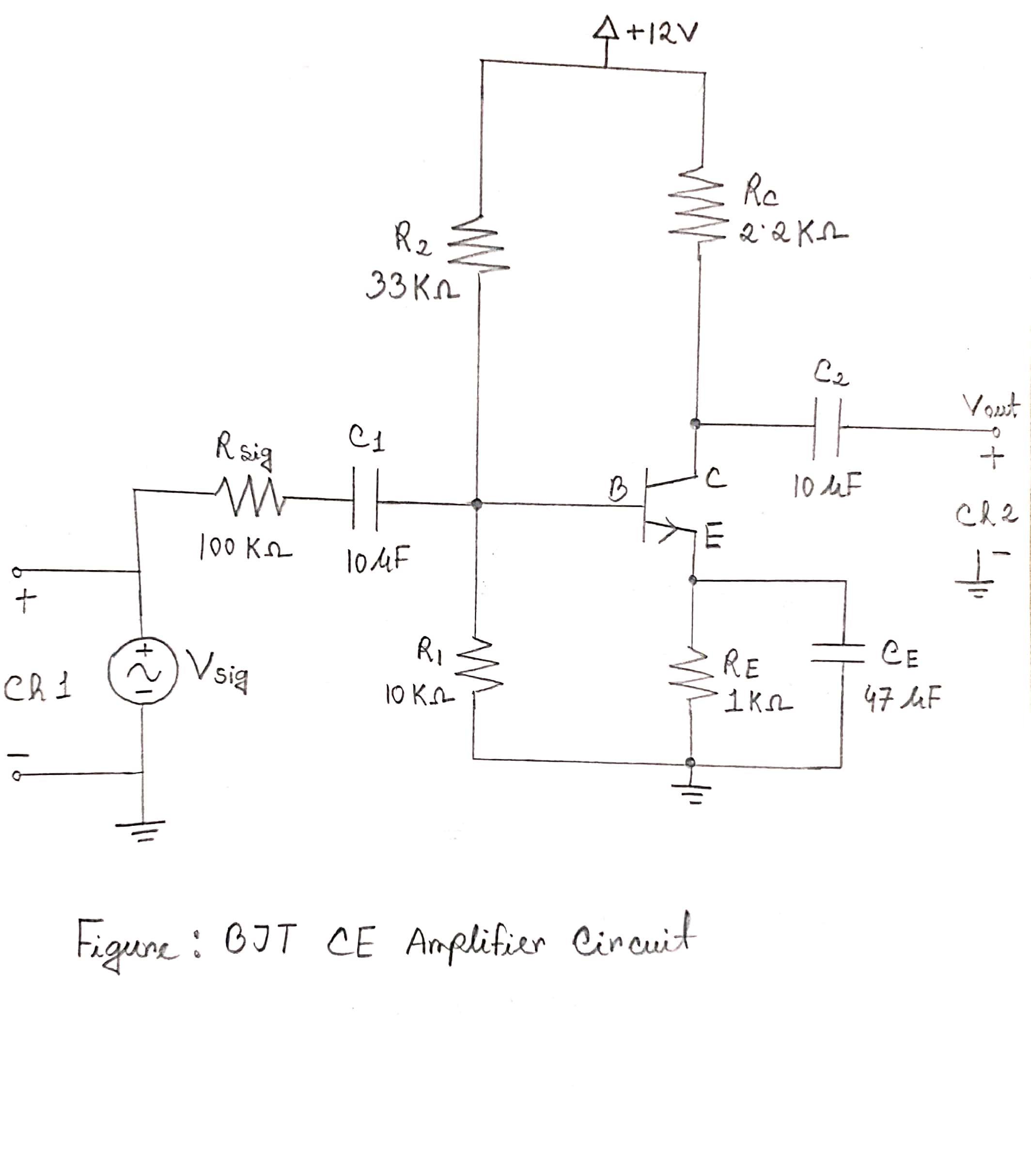
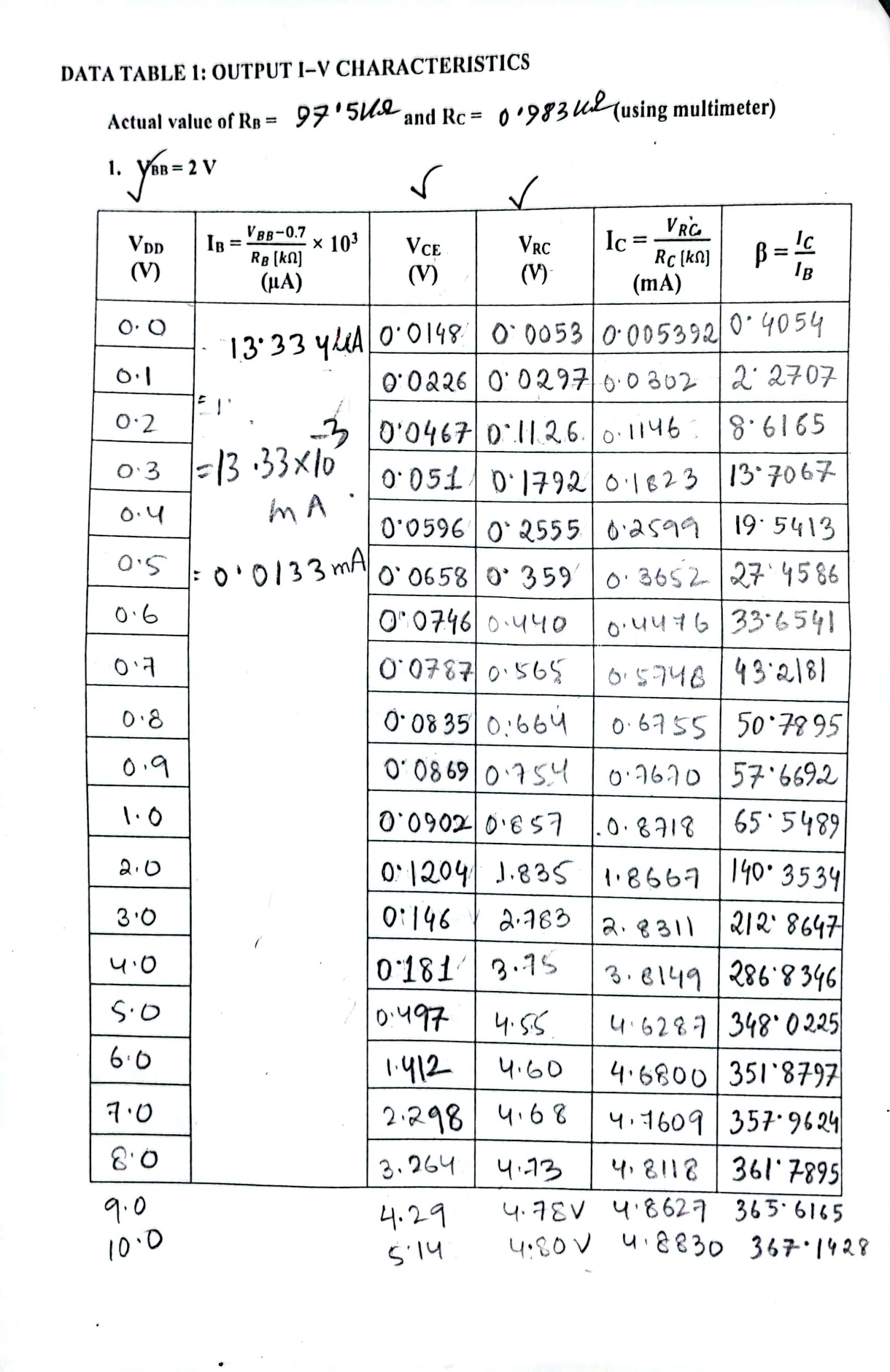
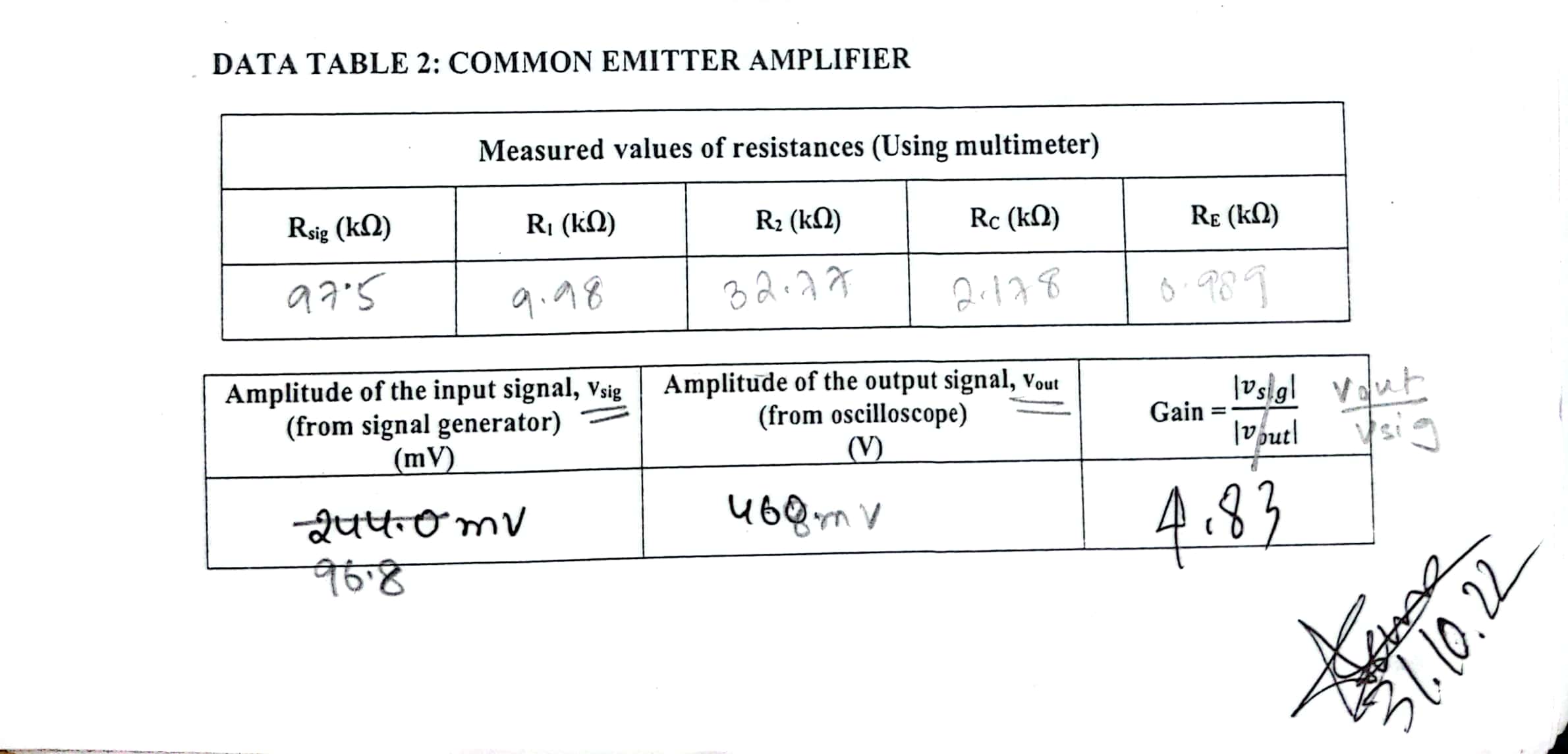
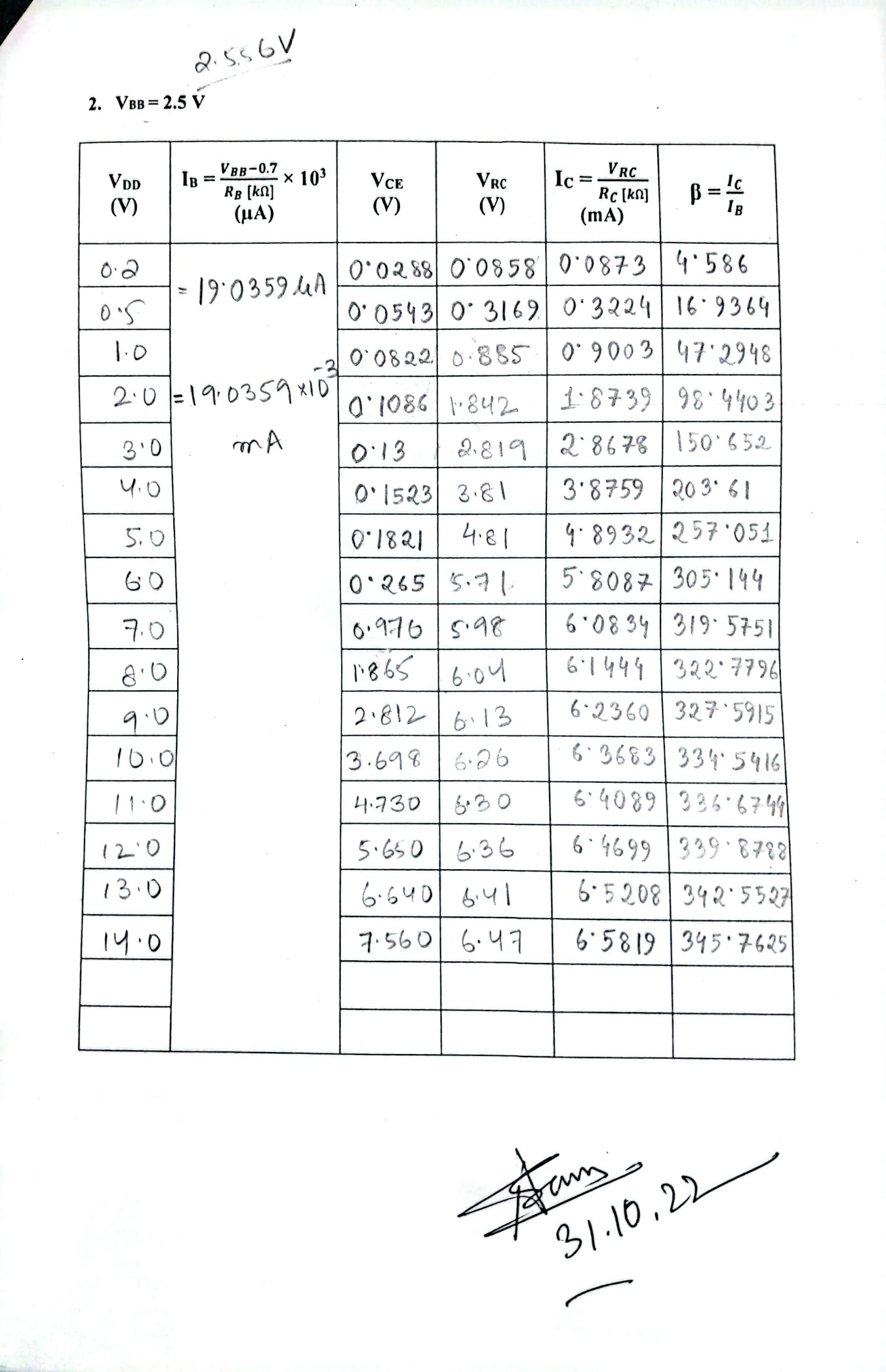


Diagram 2:



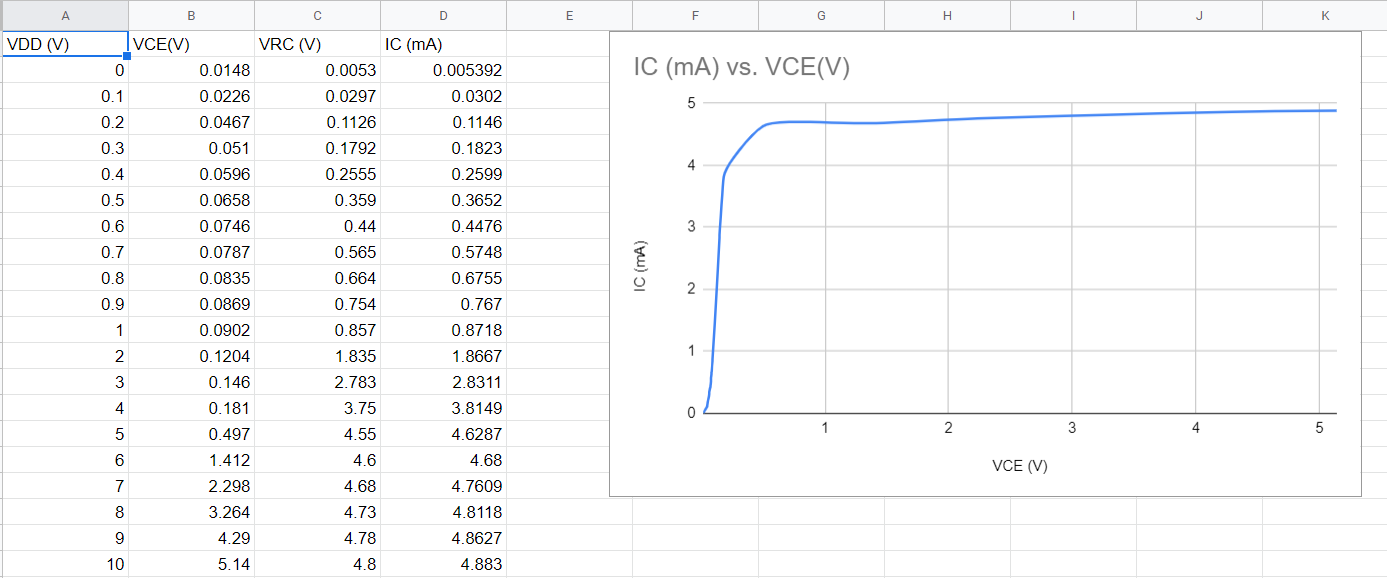
**3. Signed Data Sheets and Calculations:**

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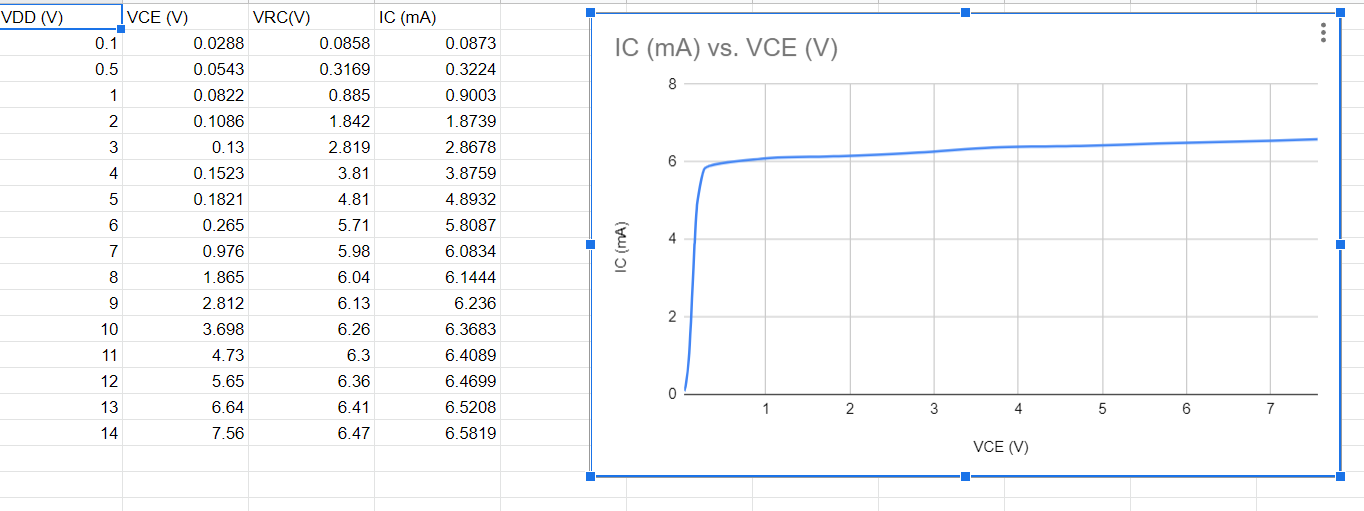
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**4. Graphs of IC vs Vce:**

For Vbb= 2v:



For Vbb= 2.5v:



**5. LT spice Circuit Diagrams:**

Diagram 1:

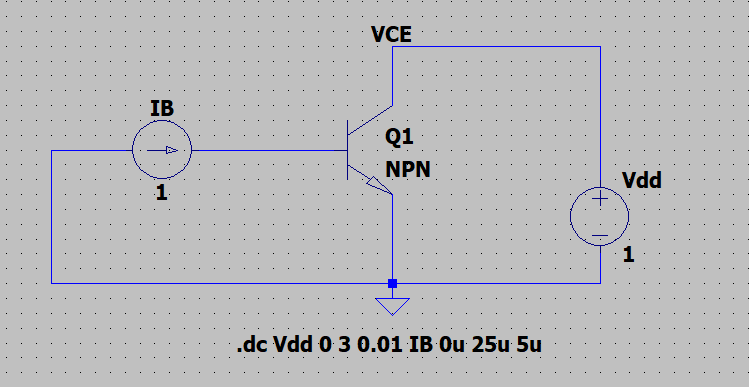
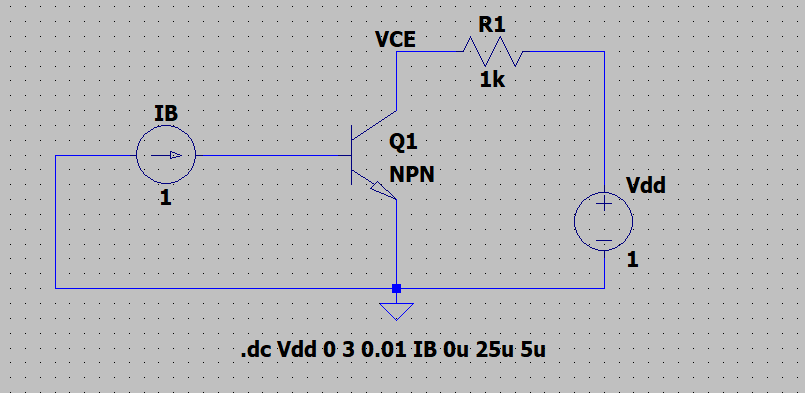
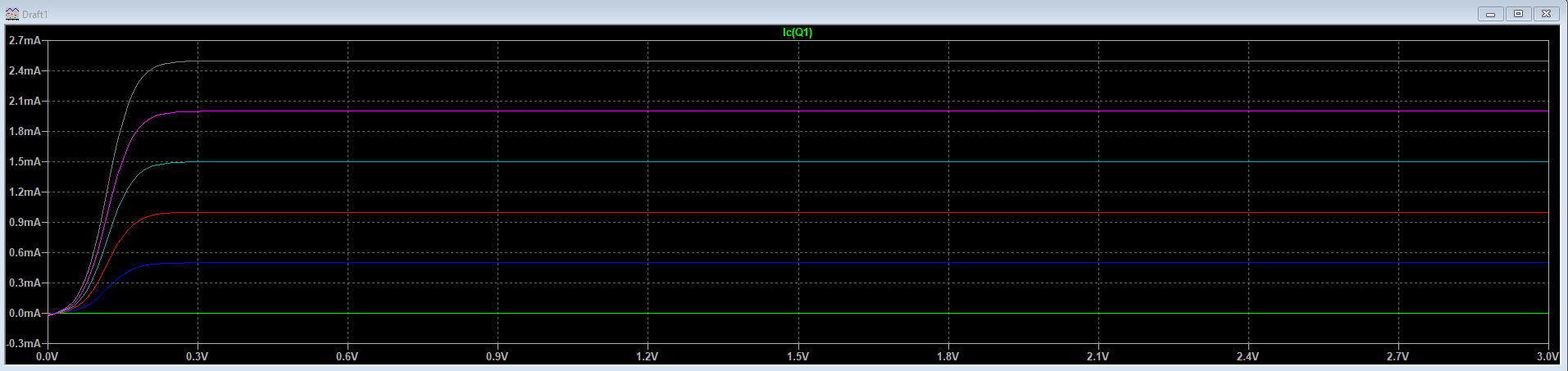


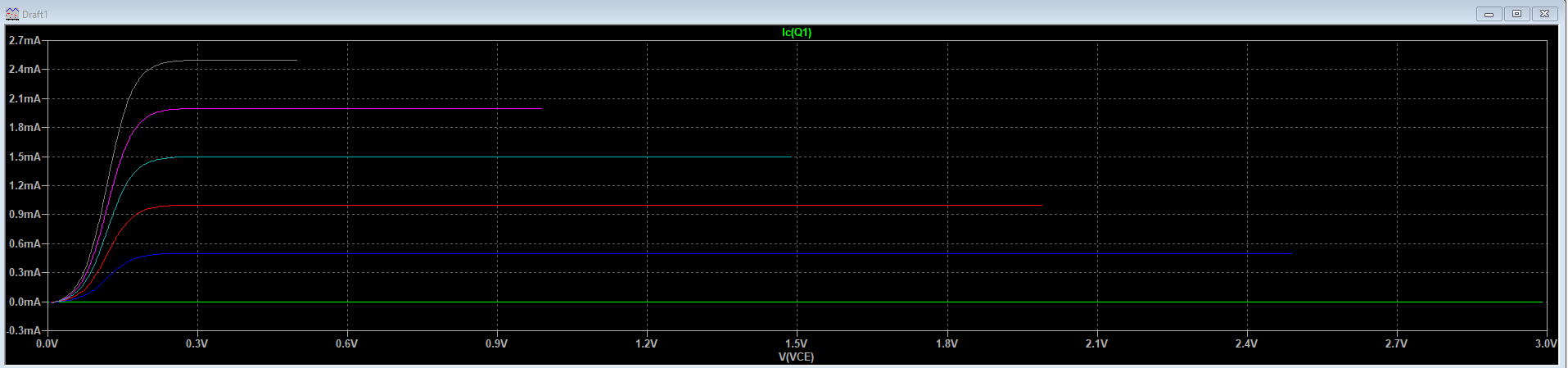
Diagram 2:



**6. Plots Generated in LT spice simulation:**

Plot 01:

Plot 2:



**7. Discussion:**

IC varies with changes in Vce while IB is held constant, as seen by the I-V characteristics produced from the datasets of the hardware experiment of circuit 1. We can observe from the graph that it was created that the collector current starts off rapidly increasing until becoming almost constant. Three regions can be identified on this graph: When Vce is increased by a specific amount and the output current stays the same, this region is known as the active region. Second, the saturation region, where IC rapidly increases from 0 to the active region. Third is the Cut-off Region, where there is almost no current. The output I-V characteristics show that, in the active region, IC increases with an increase in IB if VCE is maintained constant. In fact, the relationship between IC and IB in active mode is linear, and the following equation can be used to illustrate it: IC = βIB.

In the second plot of the Lt spice diagrams, we could notice that the Ic (collector current) was not reaching the end of Vce in the plot. We know that, Vce= Vdd - Ic\*Rc. Hence, when Ib is increased Ic also increases as Ib initially passes through the BJT to provide collector current. Hence, Vce decreases due to more Ic. In the same way, when Ib is decreased, Ic is also decreased. Hence, in that case, Vce is increased. However, after a time we cannot reach our collector current for a higher Vce as it keeps decreasing.

We noticed some of the discrepancies in the hardware experiment such as some values we measured were not theoretically accurate. For some of the inputs, we measured Vce and Vrc which were not theoretically accurate. Although our final graph generated after smoothing out looked correct yet some of the data were faulty due to the human and hardware errors we usually see in hardware experiments. As per precautions, we were careful about how much voltage we were giving as input so that no device gets harmed in the process.